SST440/441

Monolithic N-Channel JFET Duals

Product Summary

Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (pA)	$\|V_{GS1} - V_{GS2}\|$ Max (mV)
SST440	−1 to −6	−25	4.5	−1	10
SST441	−1 to −6	−25	4.5	−1	20

SST441, For applications information see AN102, page 6.

Features

- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 90 dB

Benefits

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- High-Speed Performance
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

Applications

- Wideband Differential Amps
- High-Speed,Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

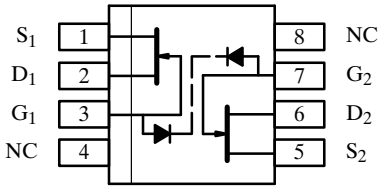
Description

The SST440/441 are monolithic high-speed dual JFETs mounted in a single SO-8 package. These JFETs are an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications.

The SO-8 package is available with tape-and-reel options to support automated assembly (see Packaging Information).

For similar products in TO-71 packaging, see the U440/441 data sheet.

Narrow Body SOIC



Top View

Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 50 mA
Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300°C
Storage Temperature . . . . . −55 to 150°C
Operating Junction Temperature . . . . . −55 to 150°C

Power Dissipation : Per Side[a] . . . . . 300 mW
Total[b] . . . . . 500 mW

Notes
a. Derate 2.4 mW/°C above 25°C
b. Derate 4 mW/°C above 25°C

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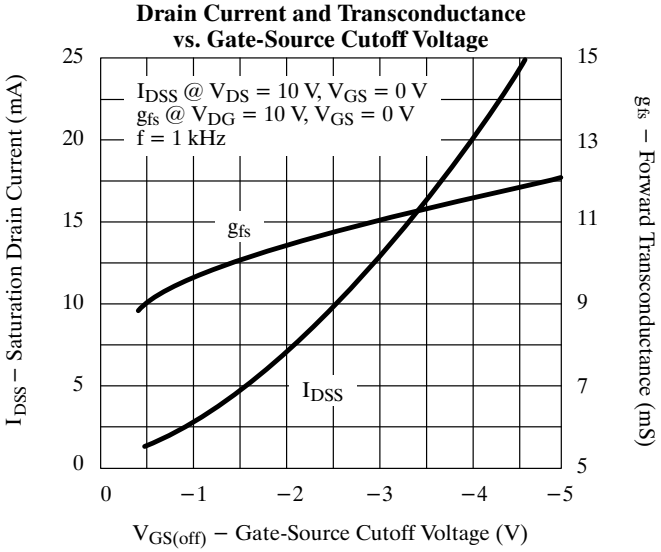
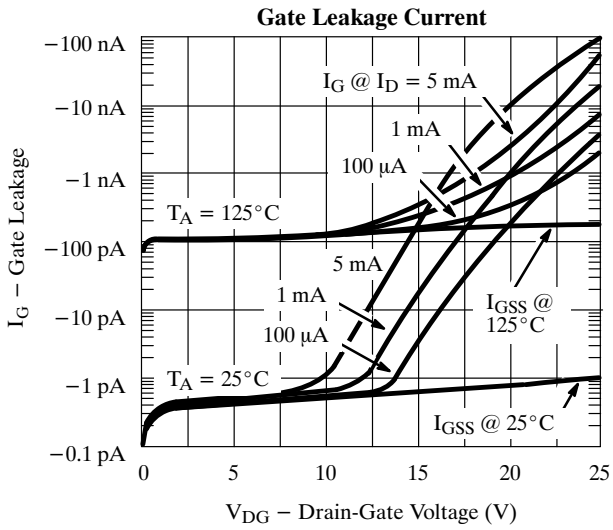
Specifications[a]

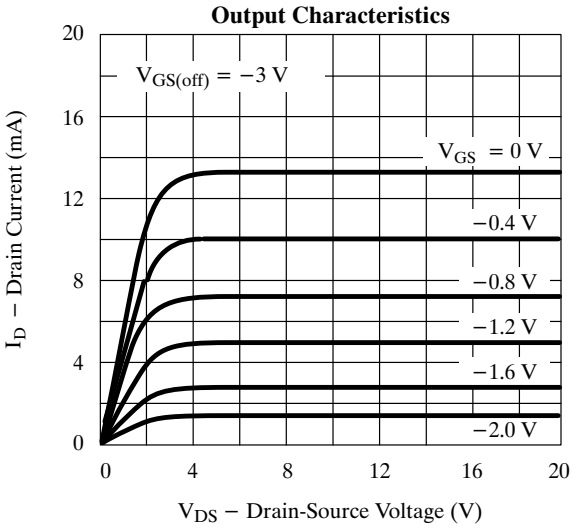
Parameter	Symbol	Test Conditions	Typ[b]	Limits SST440 Min	Limits SST440 Max	Limits SST441 Min	Limits SST441 Max	Unit
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1$ µA, $V_{DS} = 0$ V	−35	−25		−25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 10$ V, $I_D = 1$ nA	−3.5	−1	−6	−1	−6	
Saturation Drain Current[c]	I_{DSS}	$V_{DS} = 10$ V, $V_{GS} = 0$ V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -15$ V, $V_{DS} = 0$ V	−1		−500		−500	pA
		$T_A = 125°C$	−0.2					nA
Gate Operating Current	I_G	$V_{DG} = 10$ V, $I_D = 5$ mA	−1		−500		−500	pA
		$T_A = 125°C$	−0.2					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1$ mA , $V_{DS} = 0$ V	0.7					V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $I_D = 5$ mA, f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		20		200		200	µS
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $I_D = 5$ mA, f = 100 MHz	5.5					mS
Common-Source Output Conductance	g_{os}		30					µS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 10$ V, $I_D = 5$ mA, f = 1 MHz	3.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					
Equivalent Input Noise Voltage	$\overline{e}_n$	$V_{DS} = 10$ V, $I_D = 5$ mA, f = 10 kHz	4					$\frac{nV}{\sqrt{Hz}}$
Matching								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	$V_{DG} = 10$ V, $I_D = 5$ mA	7		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	$V_{DG} = 10$ V, $I_D = 5$ mA, $T_A = -55$ to 125°C	10					µV/°C
Saturation Drain Current Ratio[d]	$\frac{I_{DSS1}}{I_{DSS2}}$	$V_{DS} = 10$ V, $V_{GS} = 0$ V	0.98					
Transconductance Ratio[d]	$\frac{g_{fs1}}{g_{fs2}}$	$V_{DS} = 10$ V, $I_D = 5$ mA, f = 1 kHz	0.98					
Common Mode Rejection Ratio	CMRR	$V_{DG} = 10$ to 15 V, $I_D = 5$ mA	90					dB

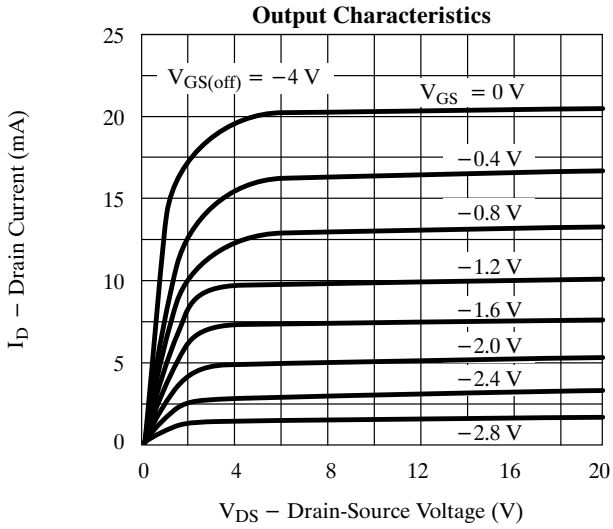
Notes
a. $T_A = 25°C$ unless otherwise noted. NNZ
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Pulse test: PW ≤ 300 µs duty cycle ≤ 3%.
d. Assumes smaller value in the numerator.

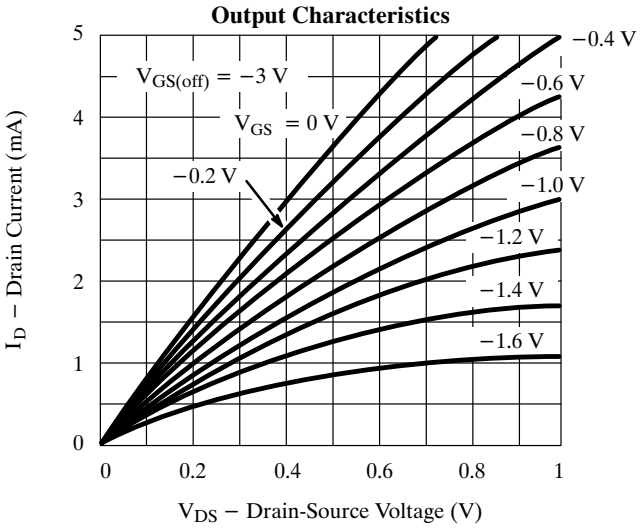
Typical Characteristics

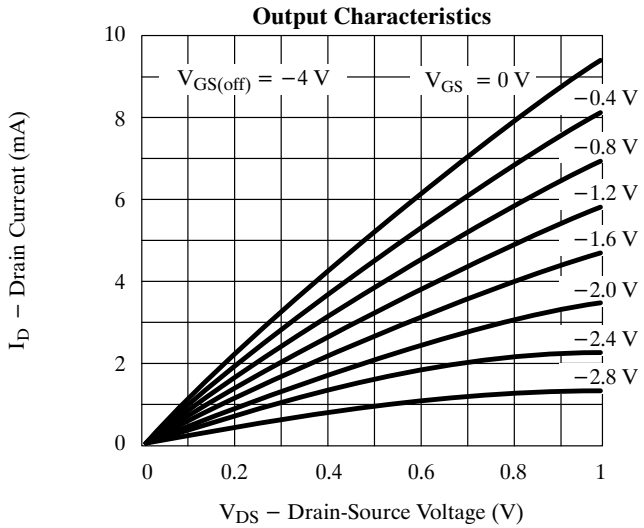












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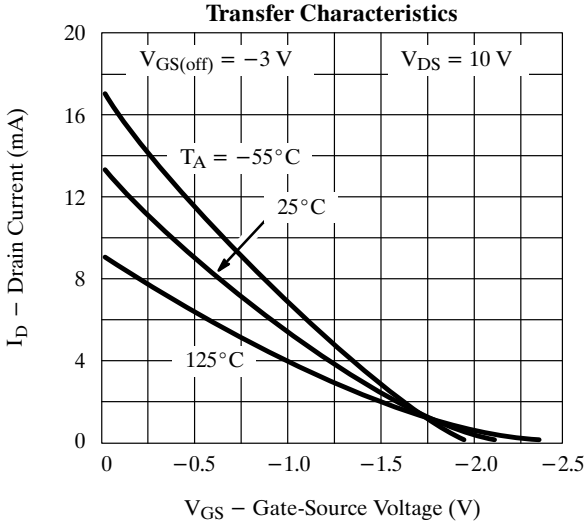
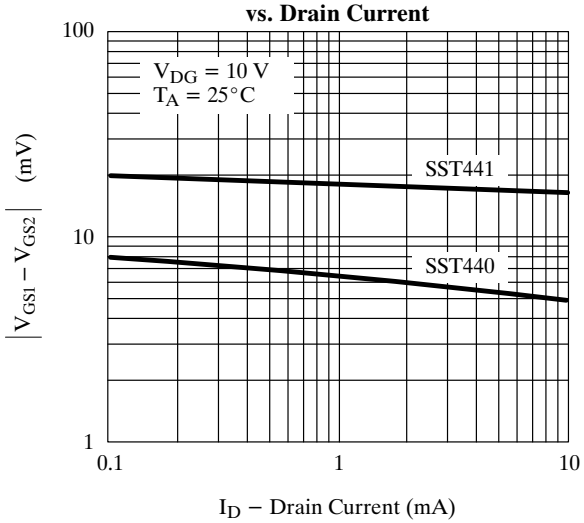
Typical Characteristics (Cont'd)

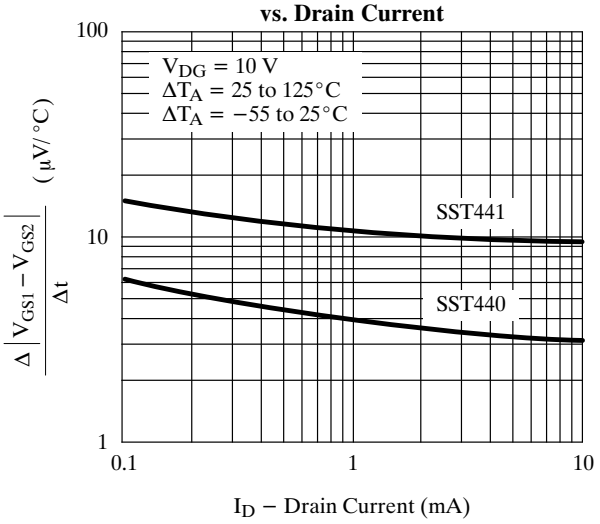
Transfer Characteristics



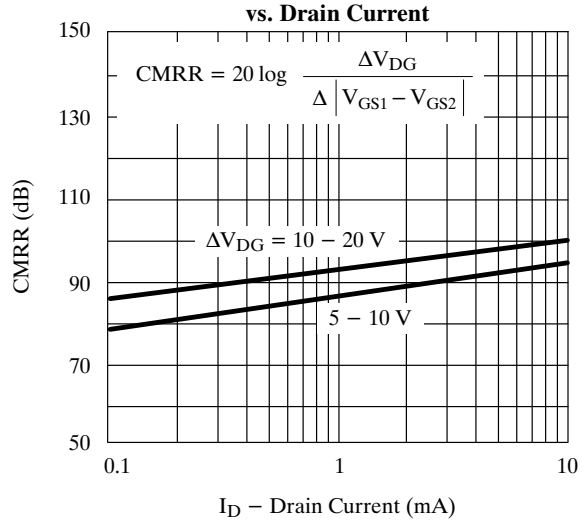
Gate-Source Differential Voltage vs. Drain Current



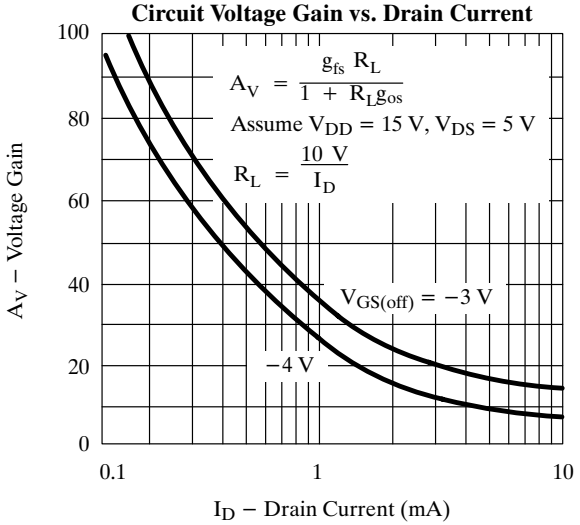
Voltage Differential with Temperature vs. Drain Current



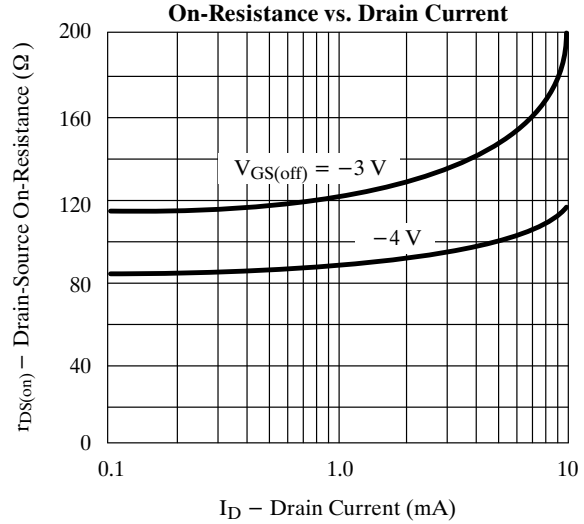
Common Mode Rejection Ratio vs. Drain Current



Circuit Voltage Gain vs. Drain Current

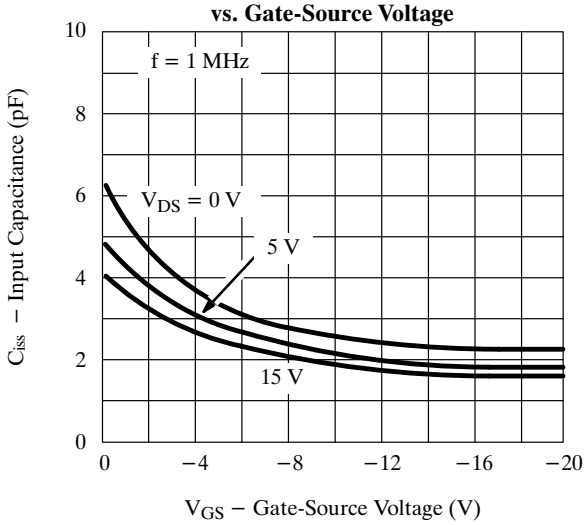


On-Resistance vs. Drain Current

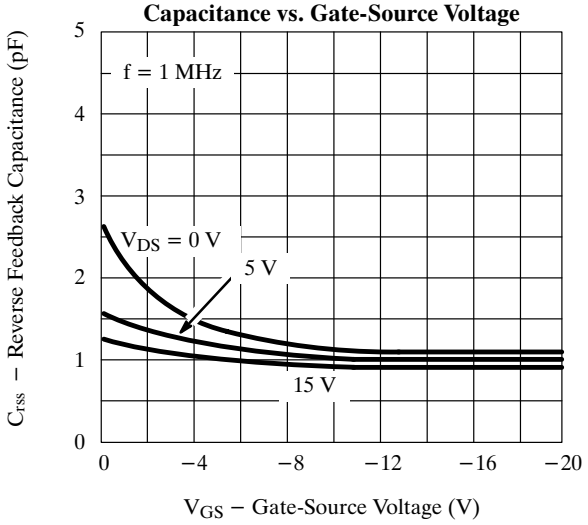


Typical Characteristics (Cont'd)

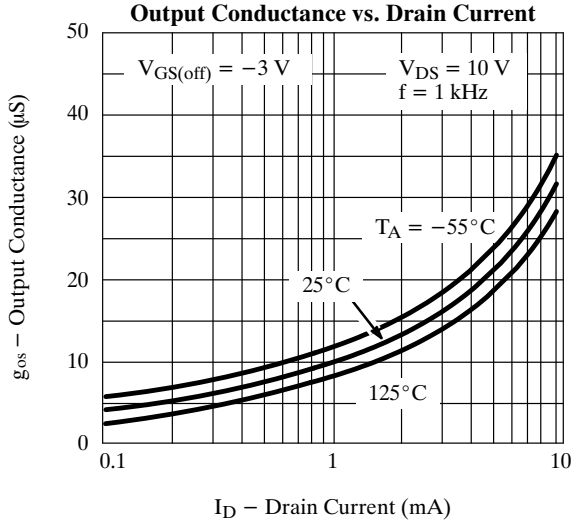
Common-Source Input Capacitance vs. Gate-Source Voltage



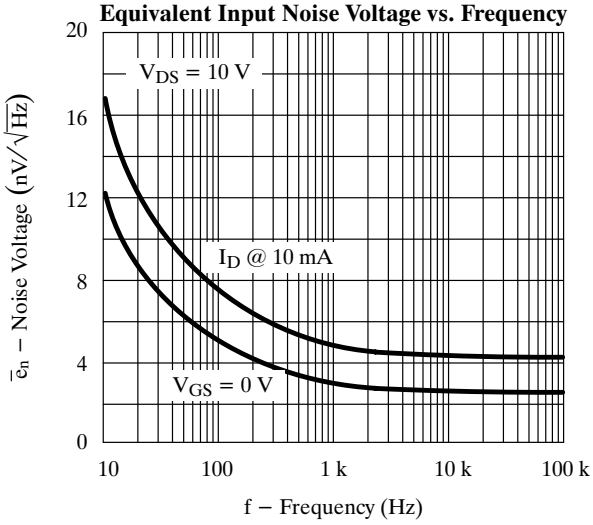
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



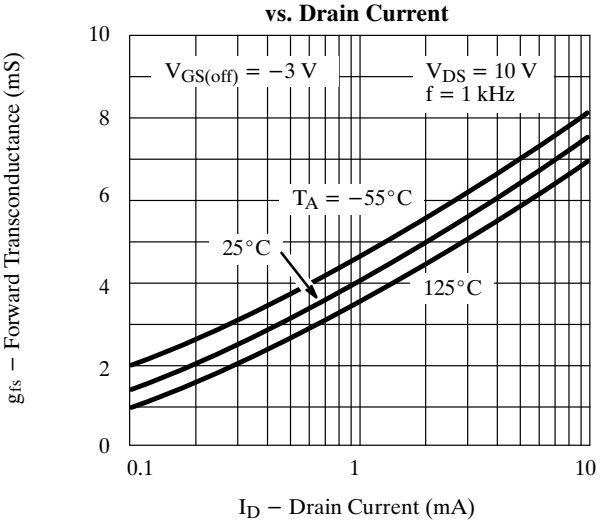
Output Conductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



Common-Source Forward Transconductance vs. Drain Current



On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage